REMARKS

Claims 1-29 were pending and presented for examination and in this application. In an Office action dated June 14, 2006, claims 1-29 were rejected. Applicants thank Examiner for examination of the claims pending in this application and addresses Examiner's comments below.

Applicants are amending claims 1, 4, 6, 13, 15, 16, and 23 in this Amendment and Response. These changes are believed not to introduce new matter, and their entry is respectfully requested. In making these amendments, Applicants do not concede that the subject matter of such claims was in fact disclosed or taught by the cited prior art. Rather, Applicants reserve the right to pursue such protection at a later point in time and merely seeks to pursue protection for the subject matter presented in this submission.

In view of the Amendments herein and the Remarks that follow, Applicants respectfully request that Examiner reconsider all outstanding rejections, and withdraw them.

Response to Rejection Under 35 USC § 112, Paragraph 2

In the 1st paragraph of the Office action, Examiner has rejected claim 6 under 35 USC § 112, ¶ 2 as allegedly not specifically pointing out and distinctly claiming the subject matter that the Applicants regard as the invention.

Applicants have amended claim 6 to recite:

> … the redundant memory element replaces the first column or the second column only if one or more fails are counted in the first column or the second column.

The amended claim no longer contains a negative limitation and distinctly claims the subject matter which Applicants regard as the invention. This amendment has been made to

improve readability of the claims, and does not narrow the scope of protection with respect to the prior art, or with respect to potentially infringing devices/compositions/articles.

Response to Rejection Under 35 USC 102(e) in View of Hughes

In the 3rd paragraph of the Office Action, Examiner rejects claims 1-29 under 35 USC § 102(e) as allegedly being anticipated by U.S. Patent No. 6,373,758 to Hughes et al. ("Hughes"). This rejection is now traversed.

Representative claim 1 has been amended to recite a method comprising:

> counting fails in the first memory element with a counter;
>
> counting fails in the second memory element with the counter;
>
> comparing the number of fails in the first memory element to the number of fails in the second memory element;
>
> determining the one of the first memory element and the second memory element having the most fails; and
>
> allocating a redundant memory element to replace the one of the first memory element and the second memory element having the most fails.

The claimed invention provides a method for efficiently counting failures in a memory and repairing the failures using redundant memory elements. The method counts the number of fails in each memory element, compares the number of fails in each memory element to determine the memory element having the most fails, and allocates a redundant memory element to replace the memory element with the most fails. The method advantageously allows the replacement determination to be made in only a single pass through BIST. The claimed invention can thus avoid wasted test cycles and can repair memory cells more quickly than with an iterative method.

The cited reference does not disclose, teach or suggest the claimed invention. Hughes discloses a method for eliminating faulty memory cells in a memory array with replacement columns of memory cells and replacement rows of memory cells. However, Hughes teaches an "iterative approach to detecting and immediately initiating repairs." (Hughes, column 6, lines 7-10). In Hughes, the number of faulty cells in a memory element is compared against a threshold value to determine whether the memory element should be replaced. If the number of faults in each memory element is less than the threshold, the threshold is decremented and the process repeats. Hughes only discloses comparing the number of faulty cells against a threshold value and fails to disclose the claimed step of "comparing the number of fails in the first memory element to the number of fails in the second memory element." The iterative method of Hughes is inefficient because extra BIST passes are needed to repair a cell if the number of fails is lower than the current threshold value.

In view of at least the above amendments and remarks, Applicants respectfully submit that claim 1 is patentably distinguishable over Hughes. Likewise, the reasons set forth above are applicable to independent claims 15, 16, and 23. Thus, Applicants request reconsideration and withdrawal of the rejection to claims 1, 15, 16, and 23. In addition, Applicants request allowance of these claims at this time.

Claims 2-14, 17-22, and 24-29 are directly or indirectly dependent on claims 1, 16, and 23. These claims are patentably distinguishable over the cited reference for at least the same reasons as the independent claims. Further, the dependent claims contain additional patentable matter. For example, dependent claim 13 recites a method comprising:

> ...testing the redundant column to determine a number of failing bits;

determining if the redundant column has less fails than one of the plurality of columns with the greatest number of failing bits; and

allocating the redundant column to replace the one of the plurality of columns with the greatest number of failing bits if the redundant column has fewer failing bits.

The claimed method tests the redundant memory element and replaces the memory element with the most fails if the redundant memory element has fewer fails. The method advantageously ensures that more fails are not introduced into the memory array by a replacement. This provides a more efficient test and repair procedure than in an iterative system because it does not require multiple passes of BIST.

Hughes discloses that replacement columns contain untested cells. However, in addressing this issue, Hughes teaches a method of running "a second pass of BIST" (column 10, lines 29-48) to ensure that replacement cells operate properly. Thus, Hughes uses an iterative approach of comparing the number of fails to a threshold value. Hughes makes a replacement without testing first and does not disclose the step of "determining if the redundant column has less fails than one of the plurality of column with the greatest failing bits". Thus, Hughes is deficient because it teaches an inefficient iterative approach that requires multiple passes of BIST to properly replace failed memory elements. Therefore, Applicants respectfully submit that claim 13 is patentably distinguishable over the cited reference. Removal of the basis of the rejection to this, and the other, dependent claims is requested.

Conclusion

In sum, Applicants respectfully submit that claims 1-29, as presented herein, are patentably distinguishable over the cited reference. Therefore, Applicants request reconsideration of the basis for the rejections to these claims and request allowance of them.

In addition, Applicants respectfully invite Examiner to contact Applicants' representative at the number provided below if Examiner believes it will help expedite furtherance of this application.

Respectfully Submitted,
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